IIT Mandi

Approval: 14th senate meeting

Course Number	**:** EE523
Course Name	**:** Digital VLSI Architecture Design
Credits	**:** 3-0-2-4.
Pre-requisite	**:** IC161 - Applied Electronics, EE312P-Microelectronics Circuit Design Practicum, EE208P-Digital System-Design Practicum or Equivalent
Intended for	**:**Final year BTech Electrical Engineering (EE), MS, M. Tech. & PhD.
Distribution	**:** Elective for Final year B. Tech (EE), MS, M. Tech. & PhD
Semester	**:** Even or Odd.

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1. Preamble:

This course has been design to compressively understand the digital architectural designs of very-large scale-integration (VLSI) systems as seen in complex system-on-chips (SoCs). It delivers overall understanding of VLSI architectures compliant to signal processing/communication systems and sub-systems with the notion of optimization for area, speed, power dissipation, cost and reliability. Additionally, it emphasizes on the architectural design of array systems and its use in various applications. It will encompass within its folds traditional and state of the art digital VLSI architectures optimized for specific purposes.

2. Course Modules with Quantitative Lecture Hours:

1. **Introduction:** Review of VLSI design flow, goals of VLSI design: optimization of speed, power dissipation, cost and reliability. **[2 hours]**

2. **System Design Flow & Fixed-point Arithmetic:** Overview, system design flow, representation of numbers, floating point format, *Qn.m* format for fixed point arithmetic, floating-point to fixed-point conversion, block floating-point formats, forms of digital filters. **[2 hours]**

3. **Algorithm to Architecture Transformation:** Architectural antipodes, transform approach to VLSI architectures, graph based formalism for describing processing algorithms, isomorphic architecture. **[3 hours]**

4. **Equivalence Transforms for Combinational Computations:** Common assumptions, pipelining, replication, time sharing, associatively transform and other algebraic transforms. **[5 hours]**

5. **Clocking of Synchronous Circuits:** Single-phase and two-phase clocking, wave pipelining, collective clock-buffer design, distributed clock-buffer trees, hybrid-clock distribution networks, impact of clock distribution delay on input/output (I/O) timing. **[6 hours]**

6. **Asynchronous Data Processing Architectures:** Data consistency problem of vectored acquisition-plain bit parallel synchronization, unit distance coding, suppression of cross

patterns, handshaking, partial handshaking, data consistency problem of scalar acquisition-synchronization at single place, synchronization at multiple places, synchronization from a slow clock, meta-stable synchronizer behavior. **[5 hours]**

7. **Digital Signal Processing Using Array Architectures:** Systolic and wave-front arrays, mapping dependence and signal flow graphs to systolic and wave-front arrays, asynchronous communication protocols for wave-front arrays. **[5 hours]**

8. **Architectural Synthesis and Optimization:** Circuit specifications for architectural synthesis, fundamental architectural synthesis problems, temporal domain-scheduling, spatial domain-binding, sequencing graphs, hierarchical models, synchronization problem, area and performance estimation, data path and control unit synthesis, constrained and unconstrained scheduling, scheduling of pipelined circuits. **[8 hours]**

9. **CORDIC Based Architectures:** Introduction, CORDIC algorithm for hardware implementation, hardware mapping, time-shared architecture, C-slow time shared architecture, modified CORDIC algorithm, recording of binary representation as ±1, hardware optimization, optimal hardware design for CORDIC. **[2 hours]**

10. **Digital Design of Communication Systems**: Top-level design options: bus-based design, point-to-point design, network-based design, hybrid connectivity, point-point KPN-based top-level design, KPN with shared bus and DMA controller, network-on-chip (NoC) top-level design, design of a router for NoC, run-time configuration, NoC for software defined radio. Typical digital communication system: source encoding, data compression, encryption, channel coding, framing, modulation, digital up-conversion and mixing, front end of the receiver. **[4 hours]**

3. Text Books:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press (2009).

2. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw Hill (2012).

4. References:

1. A.M. Fahim, "Clock generators for SoC processors: Circuits and Architectures", Kluwer Academic Publishers (2005).

2. Magdy A. Bayoumi, "VLSI Design Methodologies for Digital Signal Processing Architectures", Springer (2012).

3. Shoab Ahmed Khan, "Digital Design of Signal Processing Systems – A Practical Approach", Wiley (2011).

4. S.Y. Kung, "VLSI Array Processors", Prentice Hall (2012).