Approval: 14th Senate Meeting

Course Number	**:** EE524
Course Name	**:**Digital MOS LSI Circuits
Credits	**:** 3-0-0-3.
Pre-requisite	**:** IC161 - Applied Electronics or Equivalent, EE311-Device Electronics for Integrated Circuits or Equivalent
Intended for	**:**BTech Electrical Engineering (EE), M. Tech., MS & PhD.
Distribution	**:** Elective for Third and Final year B. Tech (EE), MS, M. Tech. & PhD
Semester	**:** Even or Odd.

---

1. Preamble:

The main objective of this course is to teach the students to analyze and synthesize digital logic CMOS circuits of LSI complexity. The students will learn the theory for designing digital logic circuits and logic system designs. The course would help the student to formulate and use the computational models to solve problems of physical design types which includes the development of geometric floor plan for the physical layout for the architecture of the circuit design. The course aims to give exercise and IC project design by which the students learn to manage a computer based graphic editor for physical circuit layouts and to verify the design behavior specification using a simulator.

2. Course Modules with Quantitative Lecture Hours:

1. **Introduction:** An overview of IC development and trends. A review of basic properties of MOS transistors and device physics relevant for digital logic design. CMOS process technology, layout and design rules. **(5 hours)**

2. **CMOS Inverter:** Static CMOS inverter, static behavior – switching threshold, noise margin, robustness. Dynamic behavior capacitance computation, propagation delay- first order analysis, power, energy and energy delay. **(3 hours)**

3. **Combination logic gates in CMOS:** Static CMOS design – complementary CMOS, Ratioed Logic, Pass transistor logic- dynamic CMOS Design – dynamic logic principles, speed and power dissipation, issues in dynamic design, cascading dynamic gates, designing logic for reduced supply voltage, simulation and layout techniques for complex gates. **(5 hours)**

4. **Sequential logic circuits in CMOS:** Timing metrics for sequential circuits, memory element classifications, static latches and Registers, dynamic latches and Registers, Alternative register styles – pulse and sense amplifier based registers, pipelining, Non Bi stable sequential Circuits, Choosing clock strategy. **(5 Hours)**

5. **Design Criteria: Introduction –** Custom, semi custom and structured array design approaches, cell based Design methodology, Array based implementations – pre-diffused – pre-wired arrays, characterizing logic and sequential cells **(5 Hours)**

6. **Interconnect:** Coping with interconnect , capactiveparasitics – cross talk, resistive parasitics – Ohmic voltage drop- electromigration-RC delay, inductive parasitics – voltage drop – transmission line effects, advanced interconnect techniques – reduced Swing Circuits – Current – mode transmission Techniques. **(4 hours)**

7. **Timing issues:** Timing classification of digital systems, synchronous interconnect, Synchronous timing basics, source of skew and jitter, clock distribution techniques and latch based clocking, self timed circuit design- clock synthesis and synchronization using a phase Locked loop **(5 hours)**

8. **Design verification:**Datapaths in digital Processor architectures, the adder, multiplier, shifter, power and speed tradeoffs in datapath structures -memory architecture and buliding blocks, memory core, peripheral cicuit, reliability and yield, power dissipation. **(5 hours)**

9. **Design for Testability:** issues in design for testability, ad hoc testing, scan based testing, boundary scan design, Built in self Test, test pattern generation, fault models. **(5 hours)**

3. Text Books:

1. Neil H.E. Weste and Harris D M, "CMOS VLSI Design: A circuit and Systems Perspective " Fourth Edition, Addison Wesley (2011).ISBN 10: 0-321-54774-8 / ISBN 13:978-0-321-54774-3

4. References:

1. Jan M. Rabaye, Digital Integrated Circuits: A Design Perspective (2nd Edition) Prentice-Hall 2003, ISBN 0-13-120764-4
2. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press (2000).
3. Sung-Mo Kang,YusufLeblebici, "Digital Integrated Circuits: Analysis and Design", McGraw-Hill, 2002, ISBN:0071196447
4. A. Chandrakasan, W. Bowhill, F. Fox, "Design of High Performance Microprocessor Circuits", IEEE Press, 2000, ISBN 078036001-X
5. John P. Uyemura, Thomson, "Chip Design for Submicron VLSI: CMOS Layout and Simulation", 1st Edition, 2005, ISBN:053446629X